Curriculum Vitae

Clark Barrett

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Research Interests

Automated reasoning, especially propositional satisfiability (SAT) and satisfiability modulo theories (SMT); Proof theory and automated proof generation and checking; Formal and semi-formal verification of hardware and software; Applications of automated reasoning to security; Verification and safety of artificial intelligence and machine learning systems; Verification of smart contracts.

Education

Ph.D.: Stanford University, 2003, Computer Science. Advisor: David L. Dill.
Thesis Title: *Checking Validity of Quantifier-Free Formulas in Combinations of First-Order Theories.*

M.S.: Stanford University, 1998, Computer Science. Advisor: David L. Dill.

B.S.: Brigham Young University, 1995, Electrical and Computer Engineering (with Honors), Computer Science, and Mathematics. Summa Cum Laude with University Honors. Minors: Physics, Music.

Appointments

Associate Professor (Research), Computer Science, Stanford University, Sept. 2016 to present.
Visiting Scientist, Google, Mountain View, CA, Jan. 2015 to July 2017.
Visiting Associate Professor, Stanford University, Sept. 2013 to Aug. 2016.
Associate Professor, Computer Science, Courant Institute, NYU, Sept. 2008 to Aug. 2016
Assistant Professor, Computer Science, Courant Institute, NYU, Sept. 2002 to 2008.

Research Group

Ph.D. Students: Andres Nötzli, Makai Mann, Caleb Donovick, Haoze Wu, Alex Ozdemir, Ying Sheng

Graduated Ph.D. Students:

- *Kshitij Bansal*, "Decision Procedures for Finite Sets with Cardinality, and Local Theories Extensions," Computer Science, New York University, 2016.
- *Wei Wang*, "Partition Memory Models for Program Analysis," Computer Science, New York University, 2016.
- *Liana Hadarean*, "An Efficient and Trustworthy Theory Solver for Bit-vectors in Satisfiability Modulo Theories," Computer Science, New York University, 2014.
- *Tim King*, "Effective Algorithms for the Satisfiability of Quantifier-Free Formulas Over Linear Real and Integer Arithmetic," Computer Science, New York University, 2014.
- *Dejan Jovanović*, "SMT Beyond DPLL(T): A New Approach to Theory Solvers and Theory Combination," Computer Science, New York University, 2012.
- *Igor Chikanian*, "Automatic Deduction for Theories of Algebraic Data Types," Computer Science, New York University, 2011.

- *Chris Conway*, "Tools and Techniques for the Sound Verification of Low-Level Code," Computer Science, New York University, 2011.
- *Yeting Ge*, "Solving Quantified First Order Formulas in Satisfiability Modulo Theories," Computer Science, New York University, 2010.
- *Ying Hu*, "Translation Validation of Loop Optimizations," Computer Science, New York University, 2005.

Postdocs and Research Scientists:

- *Ahmed Irfan*, Postdoc, 2019 - present.
- *Florian Lonsing*, Research Scientist, 2019 - present.
- *Aina Niemetz*, Postdoc, 2017 - 2019; Research Scientist, 2019 - present.
- *Mathias Preiner*, Postdoc, 2017 - 2019; Research Scientist, 2019 - present.
- *Nestan Tsiskaridze*, Research Scientist, 2020 - present.
- *Aleksandar Zeljic*, Postdoc, 2018 - present.
- *Yoni Zohar*, Postdoc, 2018 - present.
- *Cristian Mattarei*, Postdoc, 2016 - 2018.
- *Guy Katz*, Postdoc, 2016 - 2018.
- *Morgan Deters*, Postdoc, 2008-2013; Senior Research Scientist, 2013-2015.
- *Dejan Jovanović*, Postdoc, 2012-2013.

Visiting Scholars:

- *Stéphane Demri*, CNRS, 2012-2014.

Awards and Honors

Personal

Distinguished Artifact Award, International Conference on Tools and Algorithms for the Construction and Analysis of Systems, 2018.
Best Short Paper, Symposium on SDN Research, 2018.
Best Paper, Conference on Formal Methods in Computer-Aided Design, 2016.
Best Paper, International Test Conference, 2015.
ACM Distinguished Scientist, December 2014.
Haifa Verification Conference Award, October 2010.
Member, IFIP Working Group 2.3 (Programming Methodology), elected March, 2010.
IBM Software Quality Innovation Award, November 2008.
National Science Foundation CAREER award, 2007-2012.
Nominated for Miller Research Fellowship (declined), 2002.
Best Paper, Design Automation Conference, 1998.
National Science Foundation Graduate Fellowship (declined).
National Defense Science and Engineering Graduate Fellowship, 1995-1999.
Karl G. Maeser Graduate Fellowship, 1995.
Co-valedictorian, Brigham Young University, 1995.

Systems

HWMCC 2019: winner (Cosa2)
SMT-COMP 2019: winner of 13 first place trophies (of 18 possible) (CVC4);

SyGuS-COMP 2019: winner, general, PBE-BV, PBE-Strings, Inv tracks (CVC4)
SMT-COMP 2018: winner, main track (CVC4);
SyGuS-COMP 2018: winner, general, PBE-BV, PBE-Strings, and CLIA (tied) tracks (CVC4)
SMT-COMP 2017: winner, main track (CVC4);
SyGuS-COMP 2017: winner, linear-integer-arithmetic track and strings track (CVC4)
SMT-COMP 2016: winner, main track (CVC4);
SyGuS-COMP 2016: winner, linear-integer-arithmetic track (CVC4)
CASC 2015: winner, TFN division (CVC4);
SMT-COMP 2015: winner, main track (CVC4);
SyGuS-COMP 2015: winner, general track and linear-integer-arithmetic track (CVC4);
SV-COMP 2015: bronze medal, MemorySafety division (Cascade);
CASC 2014: winner, TFA division (CVC4);
SMT-COMP 2014: winner, ALIA, AUFLIA, AUFLIRA, LIA, LRA, QF_AUFBV, QF_LRA, QF_NRA, UF, UFLIA divisions (CVC4);
SMT-COMP 2012: winner, QF_UFLRA division (CVC4);
SMT-COMP 2007: winner, AUFLIRA division (CVC3);
SMT-COMP 2006: winner, AUFLIRA division (CVC3);

Systems Under Development

CVC4: An open-source SMT solver. Available at
`http://cvc4.stanford.edu/`.

Cosa2: An open-source SMT-based model checker. Available at
`https://github.com/upscale-project/cosa2`.

Marabou: An open-source verifier for neural networks. Available at
`https://github.com/NeuralNetworkVerification/Marabou`.

Previously Developed Systems

CoSA: An open-source hardware model-checker. Available at
https://github.com/cristian-mattarei/CoSA

SMT Solvers: Stanford Validity Checker (SVC), Cooperating Validity Checker (CVC), CVC Lite, CVC3

Cascade: A program verification platform. Available at
`http://cvc4.cs.stanford.edu/cascade/`.

TVOC: A Translation Validator for Optimizing Compilers. Available at
`http://cs.nyu.edu/acsys/tv`.

Teaching

New York University

Computer Systems Organization, Fall 2012, Spring 2013.
Class web page available at `http://cs.nyu.edu/web/Academic/Courses/archive.html`.

Logic and Verification, Spring 2003, Spring 2004.
2003 class web page available at `http://www.cs.nyu.edu/~barrett/courses/spr03/index.html`. 2004 class web page available at `http://cs.nyu.edu/courses/spring04/G22.3033-003/index.htm`.

Logic in Computer Science, Fall 2003, Fall 2004, Fall 2007, Fall 2008, Fall 2009.
Class web pages available at `http://cs.nyu.edu/web/Academic/Courses/archive.html`.

Programming Languages, Fall 2008, Spring 2012.
Class web pages available at `http://cs.nyu.edu/web/Academic/Courses/archive.html`.

Software Engineering, Spring 2005, Spring 2006, Spring 2007, Spring 2008.
Class web pages available at `http://cs.nyu.edu/web/Academic/Courses/archive.html`.

Topics in Automated Deduction, Spring 2007, Spring 2009.
Class web pages available at `http://cs.nyu.edu/web/Academic/Courses/archive.html`.

Stanford University

Advanced Computer Organization: Processor Architecture (EE 482), Teaching assistant, Spring 1997. Instructor: Kunle Olukotun.

Discrete Structures, Accelerated (CS 103X), Teaching assistant, Spring 2000, Winter 2001. Instructors: David Dill and John Mitchell.

Techniques for Program Analysis and Verification (CS 357), Co-instructor, Fall 2013, Fall 2015. Other instructors: Alex Aiken and David Dill.

Professional Activities

Steering Committee

FMCAD: Conference on Formal Methods in Computer-Aided Design, 2019-2020.

SMT: International Workshop on Satisfiability Modulo Theories, 2009-2012, 2014-2018.

Program/Event Chair

FMCAD: International Conference on Formal Methods in Computer-Aided Design, co-chair, 2019.

VNN: AAAI Spring Symposium on Verification of Neural Networks, co-chair, 2019.

NASA Formal Methods Symposium, co-chair, 2017.

SAT/SMT Summer School, organizer, 2014; chair, 2015.

SMT-COMP: Satisfiability Modulo Theories Competition, co-chair, 2005, 2006, 2007, 2008, 2009, 2010.

Amir Pnueli Memorial Symposium, chair, 2010.

SMT: International Workshop on Satisfiability Modulo Theories, co-chair, 2008.

Program Committees

CADE: Conference on Automated Deduction, 2017, 2019.

CAV: International Conference on Computer Aided Verification, 2006, 2008, 2009, 2016, 2018.

CPP: Conference on Certified Programs and Proofs, 2017.

DIFTS: Workshop on Design and Implementation of Formal Tools and Systems, 2011.

FMCAD: International Conference on Formal Methods In Computer-Aided Design, 2006, 2020.

FoMLAS: Workshop on Formal Methods for ML-Enabled Autonomous Systems, 2019.

FroCoS: International Symposium on Frontiers of Combining Systems, 2005, 2011, 2013, 2015.

IJCAR: International Joint Conference on Automated Reasoning, 2018.

MEMOCODE: International Conference on Formal Methods and Models for Codesign, 2009.

NFM: NASA Formal Methods Symposium, 2016.

PAAR: Workshop on Practical Aspects of Automated Reasoning, 2012, 2014.

PDPAR: Workshop on Pragmatics of Decision Procedures in Automated Reasoning, 2003, 2004, 2005, 2006.

PXTP: Workshop on Proof eXchange for Theorem Proving, 2011.

SAT: International Conference on Theory and Applications of Satisfiability Testing, 2005.

SIGDA: Ph.D. Forum at the Design Automation Conference, 2004, 2005.

SMT: International Workshop on Satisfiability Modulo Theories, 2007, 2008, 2009, 2010, 2011, 2012, 2020.

TPHOLs: International Conference on Theorem Proving and Higher Order Logics, 2004, 2005.

VMCAI: International Conference on Verification, Model Checking and Abstract Interpretation, 2008.

VSTTE: Workshop on Verified Software: Theories, Tools and Experiments, 2012.

WING: Workshop on Invariant Generation, 2012.

Referee

Conference/Workshop papers: CADE, CAV, DAC, EMSOFT, FMCAD, FroCoS, FSTTCS, IJCAR, LPAR, MEMOCODE, PAAR, PDPAR, POPL, SMT, TACAS, STACS, TPHOLs, VMCAI.

Journal papers: *ACM Computing Surveys*, *ACM Transactions on Computational Logic*, *AI Communications*, *Artificial Intelligence Journal*, *Communications of the ACM*, *Formal Aspects of Computing*, *Information and Computation*, *IEEE Transactions on Computer-Aided Design*, *Journal of Formal Methods in System Design*, *Journal of Automated Reasoning*, *Journal of the ACM*, *Journal on Satisfiability, Boolean Modeling and Computation*, *Journal of Symbolic Computation*, *Journal of Zhejiang University-Science A*, *Logical Methods in Computer Science*, *Theoretical Computer Science*.

Departmental Service (Stanford)

Awards committee, 2018-2020.
Gates 4A space coordinator, 2017-2020.
Lecturer search committee, 2018-2019.
Masters program student advisor, 2016-2020.
PhD admissions, 2016-2018.
Strategic research initiatives committee (chair), 2018-2020.

Departmental Service (NYU)

Appointments Committee, 2008-2009.
Coordinator for departmental spring showcase, 2007, 2008.
Department chair search committee, 2005-2006, 2008.
Director of Undergraduate Studies, 2009-2010.
Fellowship committee (PhD student admission and oversight committee), 2004-2008.
Graduate curriculum committee, 2006-2009.

Teaching load committee, 2006-2007.
Teaching assignments committee, 2009-2014.
Undergraduate curriculum committee, 2004-2010.
Undergraduate mentor, 2003-2008.

Other Activities

Participant at NSF workshops and panels.

One of three coordinators of the SMT-LIB initiative (see `http://www.smtlib.org`). Responsible for collecting and maintaining the library of benchmarks; chair of the SMT-LIB working group on model generation; contributor to many other aspects of the initiative.

Industry Experience

Consulting: Reservoir Labs Inc., Calypto Design Systems, Facebook, MIT Lincoln Laboratory, Mentor Graphics (formerly 0-in Design Automation).

Google, 2015 - 2017, Visiting Scientist (Domagoj Babic, host). Using SMT to find security vulnerabilities.

Intel, 1996, Summer Intern under Carl Seger. Prototyping and development of an early version of *Forte*, a formal verification tool suite.

Microsoft Research, 1993, Summer Intern under Charles Simonyi. Programmer on "Intentional Programming" project.

Publications

Conference Publications

(1) Caleb Donovick, Makai Mann, Clark Barrett, and Pat Hanrahan. Agile SMT-based mapping for CGRAs with restricted routing networks. In David Andrews, René Cumplido, Claudia Feregrino, and Marco Platzner, editors, *Proceedings of the International Conference on ReConFigurable Computing and FPGAs (ReConFig '19)*. IEEE, December 2019. Cancun, Mexico.

(2) Jiaxuan You, Haoze Wu, Clark Barrett, Raghuram Ramanujan, and Jure Leskovec. G2SAT: Learning to generate SAT formulas. In H. Wallach, H. Larochelle, A. Beygelzimer, F. d'Alché Buc, E. Fox, and R. Garnett, editors, *Advances in Neural Information Processing Systems 32 (NeurIPS '19)*, pages 10552–10563. Curran Associates, Inc., December 2019. Vancouver, Canada.

(3) Florian Lonsing, Karthik Ganesan, Makai Mann, Srinivasa Shashank Nuthakki, Eshan Singh, Mario Srouji, Yahan Yang, Subhasish Mitra, and Clark Barrett. Unlocking the power of formal hardware verification with CoSA and symbolic QED: Invited paper. In David Pan, editor, *Proceedings of the International Conference on Computer-Aided Design (ICCAD '19)*. IEEE, November 2019. Westminster, Colorado.

(4) Aina Niemetz, Mathias Preiner, Andrew Reynolds, Yoni Zohar, Clark Barrett, and Cesare Tinelli. Towards bit-width-independent proofs in smt solvers. In Pascal Fontaine, editor, *Proceedings of the* 27^{th} *International Conference on Automated Deduction (CADE '19)*, volume 11716 of *Lecture Notes in Artificial Intelligence*, pages 366–384. Springer, August 2019. Natal, Brazil.

(5) Haniel Barbosa, Andrew Reynolds, Daniel El Ouraoui, Cesare Tinelli, and Clark Barrett. Extending SMT solvers to higher-order logic. In Pascal Fontaine, editor, *Proceedings of the* 27^{th} *International Conference on Automated Deduction (CADE '19)*, volume 11716 of *Lecture Notes in Artificial Intelligence*, pages 35–54. Springer, August 2019. Natal, Brazil.

(6) Andres Nötzli, Andrew Reynolds, Haniel Barbosa, Aina Niemetz, Mathias Preiner, Clark Barrett, and Cesare Tinelli. Syntax-guided rewrite rule enumeration for smt solvers. In Mikoláš Janota and Inês Lynce, editors, *Proceedings of the* 22^{nd} *International Conference on Theory and Applications of Satisfiability Testing (SAT '19)*, volume 11628 of *Lecture Notes in Computer Science*, pages 279–297. Springer, July 2019. Lisbon, Portugal.

(7) Alex Ozdemir, Aina Niemetz, Mathias Preiner, Yoni Zohar, and Clark Barrett. DRAT-based bit-vector proofs in CVC4. In Mikoláš Janota and Inês Lynce, editors, *Proceedings of the* 22^{nd} *International Conference on Theory and Applications of Satisfiability Testing (SAT '19)*, volume 11628 of *Lecture Notes in Computer Science*, pages 298–305. Springer, July 2019. Lisbon, Portugal.

(8) Andrew Reynolds, Andres Nötzli, Clark Barrett, and Cesare Tinelli. High-level abstractions for simplifying extended string constraints in SMT. In Isil Dillig and Serdar Tasiran, editors, *Proceedings of the* 31^{st} *International Conference on Computer Aided Verification (CAV '19)*, volume 11561 of *Lecture Notes in Computer Science*, pages 23–42. Springer International Publishing, July 2019. New York, New York.

(9) Andrew Reynolds, Haniel Barbosa, Andres Nötzli, Cesare Tinelli, and Clark Barrett. CVC4SY: Smart and fast term enumeration for syntax-guided synthesis. In Isil Dillig and Serdar Tasiran, editors, *Proceedings of the* 31^{st} *International Conference on Computer Aided Verification (CAV '19)*, volume 11561 of *Lecture Notes in Computer Science*, pages 74–83. Springer International Publishing, July 2019. New York, New York.

(10) Martin Brain, Aina Niemetz, Mathias Preiner, Andrew Reynolds, Clark Barrett, and Cesare Tinelli. Invertibility conditions for floating-point formulas. In Isil Dillig and Serdar Tasiran, editors, *Proceedings of the* 31^{st} *International Conference on Computer Aided Verification (CAV '19)*, volume 11561 of *Lecture Notes in Computer Science*, pages 116–136. Springer International Publishing, July 2019. New York, New York.

(11) Guy Katz, Derek A. Huang, Duligur Ibeling, Kyle Julian, Christopher Lazarus, Rachel Lim, Parth Shah, Shantanu Thakoor, Haoze Wu, Aleksandar Zeljić, David L. Dill, Mykel J. Kochenderfer, and

Clark Barrett. The marabou framework for verification and analysis of deep neural networks. In Isil Dillig and Serdar Tasiran, editors, *Proceedings of the* 31^{st} *International Conference on Computer Aided Verification (CAV '19)*, volume 11561 of *Lecture Notes in Computer Science*, pages 443–452. Springer International Publishing, July 2019. New York, New York.

(12) M. R. Fadiheh, D. Stoffel, C. Barrett, S. Mitra, and W. Kunz. Processor hardware security vulnerabilities and their detection by unique program execution checking. In *Proceedings of the 2019 Design, Automation and Test in Europe (DATE '19)*, pages 994–999. IEEE, March 2019. Florence, Italy.

(13) E. Singh, K. Devarajegowda, S. Simon, R. Schnieder, K. Ganesan, M. Fadiheh, D. Stoffel, W. Kunz, C. Barrett, W. Ecker, and S. Mitra. Symbolic QED pre-silicon verification for automotive microcontroller cores: Industrial case study. In *Proceedings of the 2019 Design, Automation and Test in Europe (DATE '19)*, pages 1000–1005. IEEE, March 2019. Florence, Italy.

(14) Cristian Mattarei, Makai Mann, Clark Barrett, Ross G. Daly, Dillon Huff, and Pat Hanrahan. CoSA: Integrated verification for agile hardware design. In Nikolaj Bjørner and Arie Gurfinkel, editors, *Proceedings of the* 18^{th} *International Conference on Formal Methods In Computer-Aided Design (FMCAD '18)*, pages 7–11. FMCAD Inc., October 2018. Austin, Texas.

(15) Divya Gopinath, Guy Katz, Corina S. Păsăreanu, and Clark Barrett. Deepsafe: A data-driven approach for assessing robustness of neural networks. In Shuvendu Lahiri and Chao Wang, editors, *Proceedings of the* 16^{th} *International Symposium on Automated Technology for Verification and Analysis (ATVA '18)*, volume 11138 of *Lecture Notes in Computer Science*, pages 3–19. Springer, October 2018. Los Angeles, California.

(16) Andrew Reynolds, Arjun Viswanathan, Haniel Barbosa, Cesare Tinelli, and Clark Barrett. Datatypes with shared selectors. In Didier Galmiche, Stephan Schulz, and Roberto Sebastiani, editors, *Proceedings of the* 9^{th} *International Joint Conference on Automated Reasoning (IJCAR '18)*, volume 10900 of *Lecture Notes in Computer Science*, pages 591–608. Springer International Publishing, June 2018. Oxford, United Kingdom.

(17) Aina Niemetz, Mathias Preiner, Andrew Reynolds, Clark Barrett, and Cesare Tinelli. Solving quantified bit-vectors using invertibility conditions. In Hana Chockler and Georg Weissenbacher, editors, *Proceedings of the* 30^{th} *International Conference on Computer Aided Verification (CAV '18)*, volume 10982 of *Lecture Notes in Computer Science*, pages 236–255. Springer, July 2018. Oxford, United Kingdom.

(18) M. R. Fadiheh, J. Urdahl, S. S. Nuthakki, S. Mitra, C. Barrett, D. Stoffel, and W. Kunz. Symbolic quick error detection using symbolic initial state for pre-silicon verification. In *Proceedings of the 2018 Design, Automation and Test in Europe (DATE '18)*, pages 55–60. IEEE, March 2018. Dresden, Germany.

(19) Andres Nötzli, Jehandad Khan, Andy Fingerhut, Clark Barrett, and Peter Athanas. p4pktgen: Automated test case generation for P4 programs. In *Proceedings of the ACM Symposium on SDN Research (SOSR '18)*, pages 5:1–5:7. ACM, March 2018. Los Angeles, California.

(20) Cristian Mattarei, Clark Barrett, Shu yu Guo, Bradley Nelson, and Ben Smith. EMME: a formal tool for ECMAScript memory model evaluation. In Dirk Beyer and Marieke Huisman, editors, *Proceedings of the* 24^{th} *International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS '18)*, volume 10806 of *Lecture Notes in Computer Science*, pages 55–71. Springer, April 2018. Thessaloniki, Greece.

(21) Andrew Reynolds, Cesare Tinelli, Dejan Jovanović, and Clark Barrett. Designing theory solvers with extensions. In Clare Dixon and Marcelo Finger, editors, *Proceedings of the* 11^{th} *International Symposium on Frontiers of Combining Systems (FroCoS '17)*, volume 10483 of *Lecture Notes in Artificial Intelligence*, pages 22–40. Springer, September 2017. Brasilia, Brazil.

(22) Baoluo Meng, Andrew Reynolds, Cesare Tinelli, and Clark Barrett. Relational constraint solving in smt. In Leonardo de Moura, editor, *Proceedings of the* 26^{th} *International Conference on Automated Deduction (CADE '17)*, volume 10395 of *Lecture Notes in Artificial Intelligence*, pages 148–165. Springer, August 2017. Gothenburg, Sweden.

(23) Guy Katz, Clark Barrett, David L. Dill, Kyle Julian, and Mykel J. Kochenderfer. Reluplex: An efficient SMT solver for verifying deep neural networks. In Rupak Majumdar and Viktor Kuncak, editors, *Proceedings of the* 29^{th} *International Conference on Computer Aided Verification (CAV '17)*, volume 10426 of *Lecture Notes in Computer Science*, pages 97–117. Springer, July 2017. Heidelberg, Germany.

(24) Eshan Singh, Clark Barrett, and Subhasish Mitra. E-QED: Electrical bug localization during post-silicon validation enabled by quick error detection and formal methods. In Rupak Majumdar and Viktor Kuncak, editors, *Proceedings of the* 29^{th} *International Conference on Computer Aided Verification (CAV '17)*, volume 10426 of *Lecture Notes in Computer Science*, pages 104–125. Springer, July 2017. Heidelberg, Germany.

(25) Burak Ekici, Alain Mebsout, Cesare Tinelli, Chantal Keller, Guy Katz, Andrew Reynolds, and Clark Barrett. SMTCoq: A plug-in for integrating SMT solvers into Coq. In Rupak Majumdar and Viktor Kuncak, editors, *Proceedings of the* 29^{th} *International Conference on Computer Aided Verification (CAV '17)*, volume 10426 of *Lecture Notes in Computer Science*, pages 126–136. Springer, July 2017. Heidelberg, Germany.

(26) Andrew Reynolds, Maverick Woo, Clark Barrett, David Brumley, Tianyi Liang, and Cesare Tinelli. Scaling up DPLL(T) string solvers using context-dependent simplification. In Rupak Majumdar and Viktor Kuncak, editors, *Proceedings of the* 29^{th} *International Conference on Computer Aided Verification (CAV '17)*, volume 10426 of *Lecture Notes in Computer Science*, pages 453–474. Springer, July 2017. Heidelberg, Germany.

(27) Wei Wang, Clark Barrett, and Thomas Wies. Partitioned memory models for program analysis. In Ahmed Bouajjani and David Monniaux, editors, *Proceedings of the* 18^{th} *International Conference on Verification, Model Checking, and Abstract Interpretion (VMCAI '17)*, pages 539–558. Springer International Publishing, January 2017. Paris, France.

(28) Guy Katz, Clark Barrett, Cesare Tinelli, Andrew Reynolds, and Liana Hadarean. Lazy proofs for DPLL(T)-based SMT solvers. In Ruzica Piskac and Muralidhar Talupur, editors, *Proceedings of the* 16^{th} *International Conference on Formal Methods In Computer-Aided Design (FMCAD '16)*, pages 93–100. FMCAD Inc., October 2016. Mountain View, California. *Best paper award.*

(29) Kshitij Bansal, Andrew Reynolds, Clark Barrett, and Cesare Tinelli. A new decision procedure for finite sets and cardinality constraints in SMT. In Nicola Olivetti and Ashish Tiwari, editors, *Proceedings of the* 8^{th} *International Joint Conference on Automated Reasoning (IJCAR '16)*, volume 9706 of *Lecture Notes in Computer Science*, pages 82–98. Springer International Publishing, June 2016. Coimbra, Portugal.

(30) Liana Hadarean, Clark Barrett, Andrew Reynolds, Cesare Tinelli, and Morgan Deters. Fine-grained SMT proofs for the theory of fixed-width bit-vectors. In Martin Davis, Ansgar Fehnker, Annabelle McIver, and Andrei Voronkov, editors, *Proceedings of the* 20^{th} *International Conference on Logic for Programming, Artificial Intelligence, and Reasoning (LPAR '15)*, volume 9450 of *Lecture Notes in Computer Science*, pages 340–355. Springer, November 2015. Suva, Fiji.

(31) David Lin, Eshan Singh, Clark Barrett, and Subhasish Mitra. A structured approach to post-silicon validation and debug using symbolic quick error detection. In *Proceedings of the* 42^{nd} *International Test Conference (ITC '15)*, pages 1–10. IEEE, October 2015. Anaheim, California. *Best paper award.*

(32) Guy Katz, Clark Barrett, and David Harel. Theory-aided model checking of concurrent transition systems. In *Proceedings of the* 15^{th} *International Conference on Formal Methods In Computer-Aided Design (FMCAD '15)*, pages 81–88. FMCAD Inc., September 2015. Austin, Texas.

(33) Tianyi Liang, Nestan Tsiskaridze, Andrew Reynolds, Cesare Tinelli, and Clark Barrett. A decision procedure for regular membership and length constraints over unbounded strings. In Carsten Lutz and Silvio Ranise, editors, *Proceedings of the* 10^{th} *International Symposium on Frontiers of Combining Systems (FroCoS '15)*, volume 9322 of *Lecture Notes in Artificial Intelligence*, pages 135–150. Springer, September 2015. Wroclaw, Poland.

(34) Andrew Reynolds, Morgan Deters, Viktor Kuncak, Clark Barrett, and Cesare Tinelli. Counterexample guided quantifier instantiation for synthesis in SMT. In Daniel Kroening and Corina S. Păsăreanu, editors, *Proceedings of the* 27^{th} *International Conference on Computer Aided Verification (CAV '15)*, volume 9206 of *Lecture Notes in Computer Science*, pages 198–216. Springer, July 2015. San Francisco, California.

(35) Kshitij Bansal, Andrew Reynolds, Tim King, Clark Barrett, and Thomas Wies. Deciding local theory extensions via E-matching. In Daniel Kroening and Corina S. Păsăreanu, editors, *Proceedings of the* 27^{th} *International Conference on Computer Aided Verification (CAV '15)*, volume 9206 of *Lecture Notes in Computer Science*, pages 87–105. Springer, July 2015. San Francisco, California.

(36) Wei Wang and Clark Barrett. Cascade (competition contribution). In Christel Baier and Cesare Tinelli, editors, *Proceedings of the* 21^{st} *International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS '15)*, volume 9035 of *Lecture Notes in Computer Science*, pages 420–422. Springer, April 2015. London, United Kingdom.

(37) Tim King, Clark Barrett, and Cesare Tinelli. Leveraging linear and mixed integer programming for SMT. In *Proceedings of the* 14^{th} *International Conference on Formal Methods In Computer-Aided Design (FMCAD '14)*, pages 139–146. FMCAD Inc., October 2014. Lausanne, Switzerland.

(38) Liana Hadarean, Clark Barrett, Dejan Jovanović, Cesare Tinelli, and Kshitij Bansal. A tale of two solvers: Eager and lazy approaches to bit-vectors. In Armin Biere and Roderick Bloem, editors, *Proceedings of the* 26^{th} *International Conference on Computer Aided Verification (CAV '14)*, volume 8559 of *Lecture Notes in Computer Science*, pages 680–695. Springer, July 2014. Vienna, Austria.

(39) Tianyi Liang, Andrew Reynolds, Cesare Tinelli, Clark Barrett, and Morgan Deters. A DPLL(T) theory solver for a theory of strings and regular expressions. In Armin Biere and Roderick Bloem, editors, *Proceedings of the* 26^{th} *International Conference on Computer Aided Verification (CAV '14)*, volume 8559 of *Lecture Notes in Computer Science*, pages 646–662. Springer, July 2014. Vienna, Austria.

(40) Wei Wang, Clark Barrett, and Thomas Wies. Cascade 2.0. In Kenneth L. McMillan and Xavier Rival, editors, *Proceedings of the* 15^{th} *International Conference on Verification, Model Checking, and Abstract Interpretation (VMCAI '14)*, volume 8318 of *Lecture Notes in Computer Science*, pages 142–160. Springer Berlin Heidelberg, January 2014. San Diego, California.

(41) Timothy King, Clark Barrett, and Bruno Dutertre. Simplex with sum of infeasibilities for SMT. In *Proceedings of the* 13^{th} *International Conference on Formal Methods In Computer-Aided Design (FMCAD '13)*, pages 189–196. FMCAD Inc., October 2013. Portland, Oregon.

(42) Dejan Jovanović, Clark Barrett, and Leonardo de Moura. The design and implementation of the model constructing satisfiability calculus. In *Proceedings of the* 13^{th} *International Conference on Formal Methods In Computer-Aided Design (FMCAD '13)*, pages 173–180. FMCAD Inc., October 2013. Portland, Oregon.

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Edited Volumes

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Refereed Workshop Publications

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Technical Reports

(103) Clark Barrett, Daniel Kroening, and Thomas Melham. Problem solving for the 21st century: Efficient solvers for satisfiability modulo theories. Technical Report 3, London Mathematical Society and Smith Institute for Industrial Mathematics and System Engineering, June 2014. Knowledge Transfer Report.

(104) Dejan Jovanović and Clark Barrett. Sharing is caring: Combination of theories. Technical Report TR2011-940, Depatrment of Computer Science, New York University, October 2011.

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(108) Clark Barrett, Robert Nieuwenhuis, Albert Oliveras, and Cesare Tinelli. Splitting on demand in SAT Modulo Theories. Technical Report 06-05, Department of Computer Science, University of Iowa, August 2006.

(109) Clark Barrett, Igor Shikanian, and Cesare Tinelli. An abstract decision procedure for satisfiability in the theory of recursive data types. Technical Report TR2005-878, Department of Computer Science, New York University, November 2005.

Ph.D. Thesis

(110) Clark W. Barrett. *Checking Validity of Quantifier-Free Formulas in Combinations of First-Order Theories*. PhD thesis, Stanford University, January 2003. Stanford, California.

Book Reviews

(111) Clark Barrett. "Decision Procedures:An Algorithmic Point of View," by Daniel Kroening and Ofer Strichman, Springer-Verlag, 2008. *Journal of Automated Reasoning*, 51(4):453–456, December 2013.

Patents

(112) Subhasish Mitra, Clark Barrett, David Lin, and Eshan Singh. Post-silicon validation and debug using symbolic quick error detection, January 2020. Patent No. 10528448.

Invited Talks

"Towards Verification of Deep Neural Networks," IFIP Working Group 2.3, Los Altos, CA, October 31, 2019.

"Challenges and Opportunities in Formal Methods," Formal Methods at Scale (invitation-only NSA/DoD meeting), SRI, Menlo Park, CA, October 9, 2019.

"Upscale: Scaling up Verification for Open Source Hardware," Defense Advanced Research Projects Agency Electronics Resurgence Initiative Summit, Detroit, MI, July 16, 2019.

"Verification of Deep Neural Networks with SMT," Online Briefing for the Aerospace Vehicle Systems Institute Working Group on Machine Learning, November 13, 2018.

"Formal Methods for AI Safety," GE Edge & Controls Symposium, GE Global Research Center, Niskayuna, NY, September 27, 2018.

"Verification of Deep Neural Networks with SMT," Apple Computer Town Hall, Cupertino, CA, August 20, 2018.

"Breaking Barriers in Formal Hardware Verification," Defense Advanced Research Projects Agency Electronics Resurgence Initiative Summit, San Francisco, CA, July 24, 2018.

"Verification of Deep Neural Networks with SMT," Tutorial at the Design Automation Conference (DAC), San Francisco, CA, June 27, 2018.

"Towards Formally Verified Deep Neural Networks," High Confidence Software adn Systems Conference, Annapolis, MD, May 7, 2018.

"Formal Methods for Safe Autonomy," Workshop on The Road to Safe Autonomy, Stanford, CA, April 18, 2018.

"Towards Verification of Deep Neural Networks," NeurIPS Workshop on Machine Learning and Computer Security, Los Angeles, CA, December 8, 2017.

"Dramatic Improvements in Pre-silicon and Post-silicon Validation of Digital Systems with Quick Error Detection and Formal Methods," USC Computer Engineering Seminar, Los Angeles, CA, September 21, 2017.

"20 Years of Decision Procedures," Dill@60 Workshop, Heidelberg, Germany, July 24, 2017.

"Formal Verification of Deep Neural Networks," SystemX Workshop, Stanford, CA, April 12, 2017.

"Automatic Discovery and Localization of Tough Bugs in Large SoCs using Formal-Enhanced Quick Error Detection," DREAM Seminar, Berkeley, CA, March 6, 2017.

"Reluplex: An Efficient SMT Solver for Verifying Deep Neural Networks," Google Brain Seminar, Mountain View, CA, February 24, 2017.

"Electrical Bug Localization with Quick Error Detection Enhanced by Formal Methods," SystemX Conference, Stanford, CA, November 15, 2016.

"Satisfiability Modulo Theories," Sixth Summer School on Formal Techniques, Menlo College, Menlo Park, CA, May 23, 2016.

"Satisfiability Modulo Theories," SRI, Menlo Park, CA, November 10, 2015; Stanford University, Stanford, CA, November 11, 2015.

"The Satisfiability Revolution and the Rise of SMT," Google, New York, NY, December 9, 2014; Samsung Research America, San Jose, CA, October 7, 2014; NASA Ames, Moffett Field, CA, August 14, 2015; UC Davis, Davis, CA, May 29, 2014.

"Satisfiability Modulo Theories," Ed Clarke Symposium, Carnegie Mellon University, Pittsburg, PA, September 19, 2014.

"Proofs in Satisfiability Modulo Theories," with Pascal Fontaine and Leonardo de Moura, All about Proofs, Proofs for All, Vienna, Austria, July 18, 2014.

"SMT: Where do we go from here?" 12^{th} International Workshop on Satisfiability Modulo Theories, Vienna, Austria, July 17, 2014.

"Lazy and Eager Approaches to Solving Bit-vectors," SRC GRC CADTS Verification Review, Austin, TX, April 15, 2014.

"The Satisfiability Revolution and the Rise of SMT," ExCape Webinar, March 3, 2014, online at `https://excape.cis.upenn.edu/news-events.html`.

"Lazy Bit-Vector Solving using Subtheories," SRC GRC CADTS Verification Review, Berkeley, CA, April 10, 2013.

"Bit-Precise Reasoning in Systems Analysis and Verification," Yale University, New Haven, CT, February 14, 2013.

"The Satisfiability Revolution and the Rise of the Ingenious Machine," Stanford University, Stanford, CA, January 10, 2013.

"Scalable and Accurate SMT-based Model Checking of Data Flow Systems," AFOSR Annual Review, Washington, DC, November 27, 2012.

"Beyond DPLL(T): A New Model-Based Approach to Search in SMT and its Application to Solving Nonlinear Arithmetic," Carnegie Mellon University, Pittsburgh, PA, October 5, 2012.

"From SAT to SMT: Successes and Challenges," Harvard University, Cambridge, MA, August 19, 2012.

"New Insights on the Nelson-Oppen Method," Northeastern University, Boston, MA, August 13, 2012.

"Beyond DPLL(T): A New Boolean Search Framework for Model-Based Theory Reasoning," IFIP Working Group 2.3, Seattle, WA, July 18, 2012.

"Efficient SMT Solving for Bit-vectors and Arrays," SRC GRC CADTS Verification Review, Boulder, CO, April 11, 2012.

"Scalable and Accurate SMT-based Model Checking of Data Flow Systems," AFOSR Annual Review, Arlington, VA, October 26, 2011.

"From SVC to CVC4: 15 Years of Decision Procedures," SMT Summer School, MIT, Cambridge, MA, June 13, 2011.

"An Abstract Decision Procedure for a Theory of Bit-Vectors," SRC GRC CADTS Verification Review, Santa Barbara, CA, April 6, 2011.

"Tools and Techniques for the Sound Verification of Low-Level Code," MIT, Cambridge, MA, March 31, 2011.

"Sharing is Caring: An Efficient New Theory Combination Method," SRC GRC CADTS Verification Review, Austin, Texas, April 13, 2010.

"New Insights on the Nelson-Oppen Method," IFIP Working Group 2.3, Lachen, Switzerland, March 2, 2010.

"An Introduction to Satisfiability Modulo Theories," Tutorial (with Sanjit Seshia) at the International Conference on Computer-Aided Design (ICCAD), San Jose, CA, November 2, 2009.

"From SAT to SMT: Successes and Challenges," Keynote address at the Eighth International Workshop On The ACL2 Theorem Prover and Its Applications, Northeastern University, Boston, MA, May 12, 2009.

"Improving Bit-Vector Reasoning in Satisfiability Modulo Theories," SRC GRC CADTS Verification Review, Raleigh, NC, April 15, 2009.

"Satisfiability Modulo Theories: Successes and Challenges," NSF Workshop on Symbolic Computation for Constraint Satisfaction, Arlington, VA, November 14, 2008.

"Satisfiability Modulo Theories," MIT, Cambridge, MA, September 25, 2008.

"SAT Solvers: Theory and Practice," and "SMT Solvers: Theory and Practice," invited lectures at the Summer School on Verification Technology, Systems & Applications, Max-Planck-Institut für Informatik, Saarbrücken, Germany, September 15-19, 2008.

"SAT and SMT Solvers: Theory and Practice," MIT Lincoln Laboratory, Lincoln, MA, September 5, 2008.

"Bit-Precise Reasoning Using Satisfiability Modulo Theories," IFIP Working Group 2.3, Cambridge, UK, July 23, 2008.

"Satisfiability Modulo Theories," IBM T. J. Watson Research Center, Hawthorne, New York, May 19, 2008.

"Satisfiability Modulo Theories," UT Austin, April 18, 2008.

"Satisfiability Modulo Theories," IFIP Working Group 2.3, Santa Fe, NM, October 11, 2007.

"Satisfiability Modulo Theories in Practice," CMU, Pittsburgh, PA, April 16, 2007.

"An Abstract Decision Procedure for Satisfiability in the Theory of Recursive Data Types," Microsoft Research, Redmond, Washington, November 6, 2006.

"Satisfiability Modulo Theories," Reservoir Labs, New York, New York, October 20, 2006.

"Formal Software Verification," Cooper Union, New York, New York, October 19, 2006.

"CASCADE: C Assertion Checker and Deductive Engine," IBM T. J. Watson Research Center, Hawthorne, New York, August 31, 2006.

"Compiler Validation with Automated Decision Procedures," University of Iowa, Iowa City, Iowa, November 11, 2005.

"DPLL(T) with Generalized Theory Propagation," Workshop on Deduction and Applications, Schloß DagStuhl, October 28, 2005.

"Satisfiability Modulo Theories," Princeton University, Princeton, New Jersey, October 5, 2005.

"Theory and Practice of Decision Procedures for Combinations of Theories," invited tutorial presented with Cesare Tinelli at the 17^{th} International Conference on Computer Aided Verification (CAV '05), Edinburgh, Scotland, July 6, 2005.

"Compiler Validation using Automated Decision Procedures," Microsoft Research, Redmond, Washington, December 16, 2004.

"Compiler Validation with Automated Decision Procedures," Reservoir Labs Technical Presentation, Reservoir Labs, New York, New York, November 29, 2004; Bioinformatics Lab Talk, New York University, New York, New York, November 24, 2004; Computer Science Invited Lecture Series, Pace University, New York, New York, October 26, 2004.

"CVC Lite: Selected Stories from the Trenches," Combination of Decision Procedures Summer School, SRI International, Menlo Park, California, August 11, 2004.

"Using Proofs for Fast and Reliable Boolean Reasoning in CVC Lite," Intel Formal Verification Symposium, Hillsboro, Oregon, June 11, 2004.

"The Common Roots of Mathematics and Computing," Faculty Resource Network, New York University, New York, New York, June 8, 2004.

"Formal Software Verification," Pace University, New York, New York, March 22, 2004.

"Applying Automated Decision Procedures: Using CVC Lite in Compiler Validation," Computer Science Colloquium, Washington University, St. Louis, Missouri, September 12, 2003.

"Efficiently Combining Boolean and First-Order Reasoning," Max Planck Institut für Informatik, Saarbrücken, Germany, June 10, 2003.

"The Nelson-Oppen Method for Combining Decision Procedures," Max Planck Institut für Informatik, Saarbrücken, Germany, June 5, 2003.

"Checking Validity of Quantifier-Free Formulas in Combinations of First-Order Theories," Rice University, April 2002; University of Pisa, April 2002; California Institute of Technology, March 2002; Northrop Grumman, March 2002; NEC Laboratories, March 2002; New York University, March 2002; University of Utah, March 2002; Columbia University, March 2002; Brigham Young University, February 2002.

"A Framework for Cooperating Decision Procedures," Intel Strategic CAD Laboratories, Hillsboro, Oregon, May 2000.

"A Unified Framework for Cooperating Decision Procedures," Brigham Young University Computer Science Colloquium, Provo, Utah, March 2000.

"Bit-Vector Decision Procedures in the Stanford Validity Checker," SRI International, Menlo Park, California, May 1998.